Amendments to the Specification

[0017] An n-type silicon wafer having an original bulk spreading resistivity of about 40 ohm-cm [~~was~~] is implanted with 180 keV protons to a dose of about 3 x 10^{16} protons/cm^2 and annealed in a nitrogen-hydrogen atmosphere at 900 degrees C for 10 seconds to develop a buried hydrogen bubble or platelet layer, as further described in the Li patents. The implanted wafer [~~was~~] is annealed by heating to 1180 degrees C for 20 minutes for conversion of the top surface layer from n-type to p-type conductivity as further described in the 1996 MRS article. The surface of the annealed wafer [~~was~~] is subjected to plasma etching to reduce the thickness of the top surface layer overlying the buried layer to approximately 0.1 μm. Other suitable means for thickness reduction include chemical etching and chemical-mechanical polishing (CMP).

[0024] In operation, [~~I found that~~] the CMOS device, and in particular the NMOS portions, [~~had~~] has improved performance compared to conventional CMOS devices. Moreover, the high-resistivity p-layer [~~had~~] has significantly improved cut-off and transconductivity characteristics. Although the exact theory is not known, the SR profile appears to provide a conductivity channel through which both lateral and vertical electric fields can substantially penetrate and control charge carriers. Substantial depletion of the charge carriers [~~was~~] is obtained, thereby improving the threshold voltage and sub-threshold slope of the source-drain current. Best results are obtained by etching back the initial top surface layer until the spreading resistivity is equal to or greater than the original resistivity of the wafer.

[0026] FIG. 5 shows protons being implanted through a top surface layer 11 of an n-type wafer 13. With a first annealing step, e.g. at 900 degrees C for 10 seconds, a defect layer of platelets or bubbles is formed at or near the end of the proton range, e.g of 1.2 to 2 μm when proton energy is 180 keV and the dose is 2 x 10^{16} protons/cm^2 as described in the1996 MRS article, for example. Lower proton energies, e.g. down to 100 keV or less can be used to make thinner top surface layers 11. A second annealing step, e.g. at 1180 degrees C for 20 minutes is next applied to implanted wafer 13 in order to develop the high resistivity defect layer 12, to remove impurities from top surface layer 11 and to convert layer 11 to p-type silicon. Top

[surface layer 12] surface layer 11 is then etched and polished to reduce the thickness above defect layer 12, as described in connection with FIGS. 1 and 2, so as to fabricate an active channel for charge carriers that confines the charge carriers to a thin top surface under charge accumulation and depletion conditions and through which the gate electric field can penetrate.

[0031] In operation, the present CMOSFET device [~~showed~~] has improved transconductance and lower latch-up than conventional CMOSFET. Putatively, the improvement may be related to the combination of high-resistivity defect layer 12, which extends under all the devices, and trench 19, which electrically isolate adjacent PMOS and NMOS devices. In addition, as noted in the 1996 MRS article, improved transconductance may be attributed to the gettering action of defect layer 12 and by the etch-back step for reducing the thickness of the top surface layer. Furthermore, the spreading resistivity profile that resulted from the implantation, annealing and etch-back procedures functioned to confine the conduction of charge carriers to a thin layer 11' of the top surface layer 11 into which both normal and lateral electric fields could penetrate, thereby improving cut-off and other properties of the FET. In addition, [~~I found that~~] using wafers with minimum oxygen content [~~enabled~~] enables the defect layer 11 to getter metals and other impurities otherwise present in the top surface layer.

[0032] FIG. 9 shows schematically a view of CMOSFET fabricated on a top surface layer 91 on a defect layer 92 in a p-type Si wafer 93. The hydrogen implantation procedures are similar to those described in connection with FIG. 8 except that, as the top surface layer 91 is already p-type, implantation changes the spreading resistivity but does not change the conductivity type as described by the Li (2000) article. But, n-type dopant, such as phosphorous or arsenic [~~was~~] is implanted into channel portion 97e under gate dielectric 94a of the PMOS portion. In addition, more concentrated p+ and n+ dopants [~~were~~] are implanted into source and drain regions 97a and 97b, and 97c and 97d of the PMOS and NMOS devices, respectively. Metallic contacts 98a-98d [~~were~~] are applied to source and drain doped regions 97a-97d, and polysilicon electrodes 95a and 95b with metallic contacts 96a and 96b [~~were~~] are fabricated on gate dielectrics 94a and 94b of the PMOS and NMOS regions respectively. Deep trench 99, which penetrated defect layer 92 between the PMOS and NMOS regions, provided electrical

isolation and insulation. Again, conventional photolithographic, etching and deposition with appropriate design rules [~~were~~] are utilized.

[0033] The top surface layer 91 [~~was~~] is fabricated by controlling the annealing steps and etch back steps, such as described in connection with FIG. 1, so as to produce a spreading resistivity profile which functioned to confine the charge carriers to the top surface channel 91' of top surface layer 91. In addition, electric fields penetrated through top layer 91', thereby improving transconductance characteristics substantially compared to conventional CMOS devices. Again, metals and other impurities [~~were~~] are gettered by defect layer 92 and surface contaminants [~~were~~] are removed by etch back deeper than usual wafer processing to provide the desired SR profile.

[0039] In operation, the mobility of the charge carriers in the base [~~was found to be~~] is significantly increased compared with those in conventional bipolar and floating devices. Furthermore, when used in applications, such as logic circuits as described in the Gribnikov '245 patent, substantially improved operating characteristics [~~were~~] are found. High mobility floating base layer 101 and its defect layer 102 in contact with collector layer 103 provided unique p-n junction characteristics not heretofore available.

[0040] In addition, the improved composite epi-layer 108 on annealed and etched layer 101 on defect layer 102 [~~was found to provide~~] provides improved performance for other semiconductor devices such as, for example, described above in FIGS. 2-9. Thus such a composite is described next in connection with FIG.11.

[0042] The epitaxial layer is on the annealed and etched p-layer with the desired surface of the p-layer, after irradiating, being annealed and etched so as to produce the desired spreading resistivity. Combinations of such conductivity types include n-epi on p/peak/p or on p/peak/n, and p-epi on p/peak/p or on p/peak/n, where "peak" means the high resistivity peak which is produced by the initial defect layer. In operation [~~I found that~~], although it is necessary to create the defect layer by ion implantation in order to getter impurities and increase the resistivity above the original

resistivity of the wafer substrate, it is not necessary for a detectable defect layer to be present after annealing provided impurities are anchored at microscopic platelets or even a microscopic layer of dislocations. The crystal structure of the device region after irradiating, annealing and etching, in which devices are fabricated is improved when compared to the wafer substrate because impurities are lower in the initial surface region. Consequently the epitaxial layer, which faithfully follows its substrate structure, also has an improved crystal structure and lower impurities than available by other processes.

[0043] In operation, devices fabricated using the structure shown in FIG. 11 [~~had~~] have significantly improved electrical properties, possibly because defect layer 112 [remained] remains active in gettering impurities, thereby producing an improved crystal structure and mobility in layers 111 and 114. Such properties have never before been realized because epi-layers conventionally deposited on conventional wafers did not have the benefit of such gettering and crystal structure. Lower-cost original wafers, having higher impurity levels, can be utilized. Furthermore, when the composite structure shown in FIG. 11 is used for fabricating FET devices, the conductivity of the epitaxial layer 114 and the spreading-resistivity of p-layer 111 can be cooperatively adjusted so that charge carriers are channeled through epi-layer 114 and, in addition, latch-up between adjacent NFET and PFET devices are minimized. Such a composite layer has unique transconductance characteristics and overall device performance not available by other means.